OPENBRIX Zero

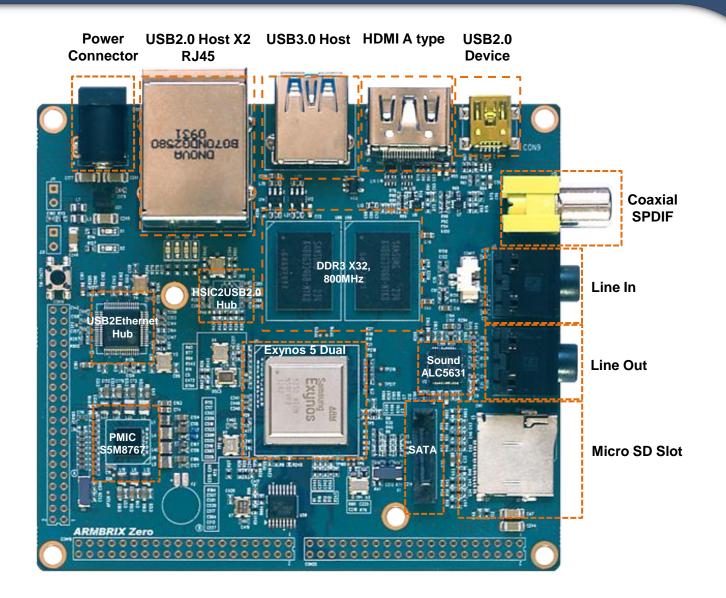
February, 2013 iAMBRIX

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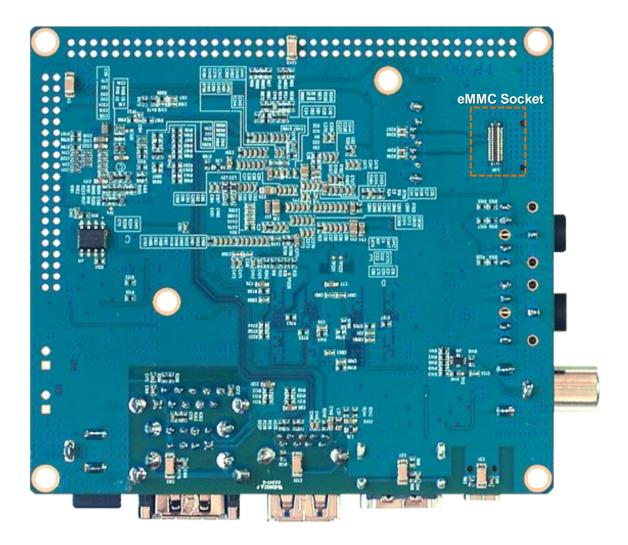
- ✓ OPENBRIX Zero specification
- ✓ OPENBRIX Zero schedule
- ✓ OPENBRIX Zero Top
- ✓ OPENBRIX Zero Bottom
- ✓ OPENBRIX Zero Extension headers



OPENBRIX Zero – Top

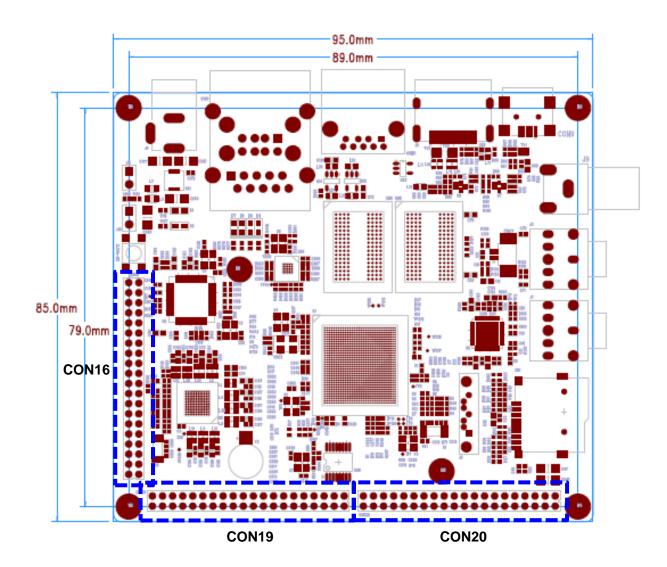


OPENBRIX Zero – Bottom



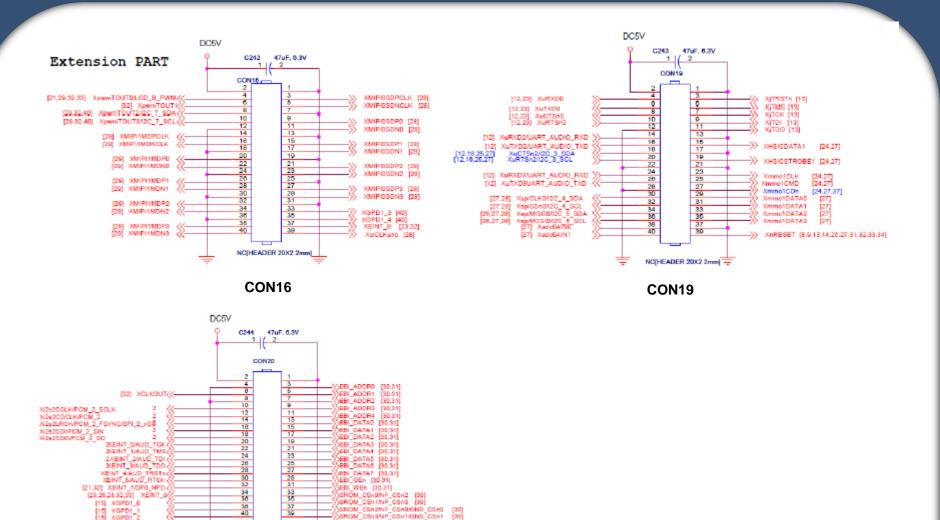


OPENBRIX Zero – Expansion Headers (1/3)





OPENBRIX Zero – Expansion Headers (2/3)



NC[HEADER 20X2 2mm]

CON20

OPENBRIX Zero – Expansion Headers (3/3)

				4 1	1	
Signal Name	Description	P/ N		Signal Name	Description	P/ N
DC5V	5V DC POWER	2		GND	Digital Ground	1
XpwmTOUT0	GPB2[0]/TOUT_0	4		XMIPI0SDPCLK	MIPI-DPHY0 slave DP clock	3
XpwmTOUT1	GPB2[1]/TOUT_1	6		XMIPI0SDNCLK	MIPI-DPHY0 slave DN clock	5
XpwmTOUT2	GPB2[2]/I2C7_SDA	8	l i	GND	Digital Ground	7
XpwmTOUT3	GPB2[3]/I2C7_SDA	10		XMIPI0SDP0	MIPI-DPHY0 slave DP data0	9
GND	Digital Ground	12		XMIPI0SDN0	MIPI-DPHY0 slave DN data0	11
XMIPI1MDPCLK	MIPI-DPHY Master clock DP	14		GND	Digital Ground	13
XMIPI1MDNCLK	MIPI-DPHY Master clock DN	16		XMIPI0SDP1	MIPI-DPHY0 slave DP data1	15
GND	Digital Ground	18	l i	XMIPI0SDN1	MIPI-DPHY0 slave DN data1	17
XMIPI1MDP0	MIPI-DPHY Master DP0	20		GND	Digital Ground	19
XMIPI1MDN0	MIPI-DPHY Master DN0	22		XMIPI0SDP2	MIPI-DPHY0 slave DP data2	21
GND	Digital Ground	24		XMIPI0SDN2	MIPI-DPHY0 slave DN data2	23
XMIPI1MDP1	MIPI-DPHY Master DP1	26		GND	Digital Ground	25
XMIPI1MDN1	MIPI-DPHY Master DN1	28	l i	XMIPI0SDP3	MIPI-DPHY0 slave DP data3	27
GND	Digital Ground	30		XMIPI0SDN3	MIPI-DPHY0 slave DN data3	29
XMIPI1MDP2	MIPI-DPHY Master DP2	32		GND	Digital Ground	31
XMIPI1MDN2	MIPI-DPHY Master DN2	34		XGPD1_3	GPD1[3]	33
GND	Digital Ground	36		XGPD1_4	GPD1[4]	35
XMIPI1MDP3	MIPI-DPHY Master DP3	38		XEINT_9	GPX1[1]/INT1[1]	37
XMIPI1MDN3	MIPI-DPHY Master DN3	40		XciXLKenb	GPH0[3]/CAM_A_CLKOUT	10

Signal Name	Description	P/ N	Signal Name	Description	P/ N
DC5V	5V DC POWER	2	GND	Digital Ground	1
RXD0	RXD0	4	J TRST	J TRST	3
TXD0	TXD0	6	J TMS	J TMS	5
CTS0	CTS0	8	J TCK	J TCK	7
RTS0	RTS0	10	J TDI	J TDI	9
GND	Digital Ground	12	J TDO	J TDO	11
RXD2	RXD2	14	GND	Digital Ground	13
TXD2	TXD2	16	HSIC1_DATA	HSIC1_DATA	15
CTS2	CTS2	18	GND	Digital Ground	17
RTS2	RTS2	20	HSIC1_STROBE	HSIC1_STROBE	19
GND	Digital Ground	22	GND	Digital Ground	21
RXD3	RXD3	24	MMC1_CLK	MMC1_CLK	23
TXD3	TXD3	26	MMC1 CMD	MMC1 CMD	25
GND	Digital Ground	28	MMC1 CDn	MMC1 CDn	27
I2C 4 SDA	IŽC 4 SDA	30	MMC1 DATA0	MMC1 DATA0	29
I2C 4 SCL	12C 4 SCL	32	MMC1 DATA1	MMC1 DATA1	31
12C 5 SDA	I2C 5 SDA	34	MMC1 DATA2	MMC1 DATA2	33
12C 5 SCL	12C 5 SCL	36	MMC1 DATA3	MMC1 DATA3	35
ADC0_0	ADC0_0	38	GND	Digital Ground	37
ADC0_1	ADC0_1	40	nRESET	nRESET	39

CON16

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Signal Name	Description	P/ N	Signal Name	Description	P/ N
DC5V	5V DC POWER	2	GND	Digital Ground	1
GND	Digital Ground	4	EBI_ADDR0	GPY3[0]/EBI_ADDR[0]	3
XCLKOUT	MAIN CLK OUT	6	EBI_ADDR1	GPY3[1]/EBI_ADDR[1]	5
GND	Digital Ground	8	EBI_ADDR2	GPY3[2]/EBI_ADDR[2]	7
XI2S2SCLK	I2S_2_SCLK	10	EBI_ADDR3	GPY3[3]/EBI_ADDR[3]	9
XI2S2CDCLK	12S_2_CDCLK	12	EBI_ADDR4	GPY3[4]/EBI_ADDR[4]	11
XI2S2LRCK	I2S_2_LRCK	14	EBI_DATA0	EBI_DATA[0]	13
XI2S2SDI	125_2_SDI	16	EBI_DATA1	EBI_DATA[1]	15
XI2S2SDO	125_2_SDO	18	EBI_DATA2	EBI_DATA[2]	17
XEINT_0	INT_0	20	EBI_DATA3	EBI_DATA[3]	19
XEINT 1	INT 1	22	EBI DATA4	EBI DATA[4]	21
XEINT 2	INT 2	24	EBI DATA5	EBI DATA[5]	23
XEINT 3	INT 3	26	EBI DATA6	EBI DATA[6]	25
XEINT 4	INT 4	28	EBI DATA7	EBI DATA[7]	27
XEINT 5	INT 5	30	EBI OEn	EBI OEn	29
XEINT 7	INT 7	32	EBI WEn	EBI WEn	31
XEINT 8	INT 8	34	EBI CSn0	EBI CSn0	33
XGPD1 0	GPD1 0	36	EBI CSn1	EBI CSn1	35
XGPD1 1	GPD1 1	38	EBI CSn2	EBI CSn2	37
XGPD1_2	GPD1_2	40	EBI_CSn3	EBI_CSn3	39

CON20

