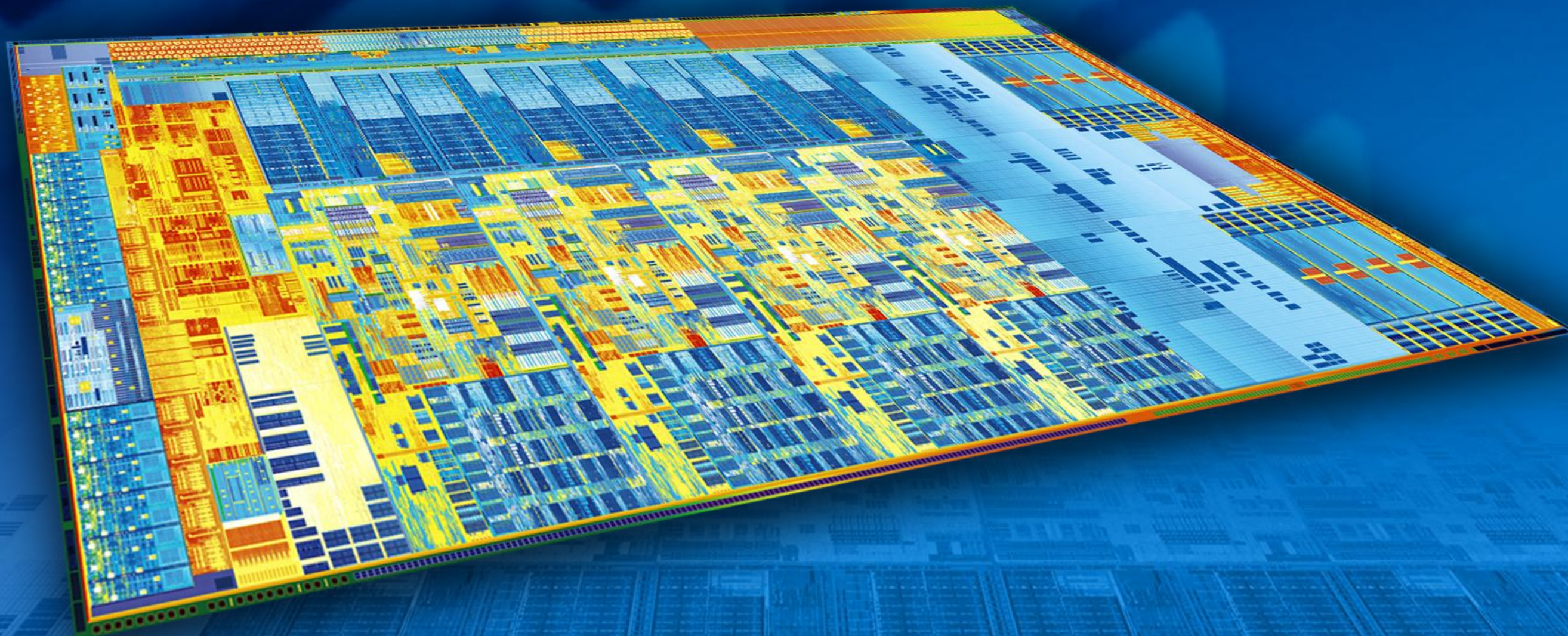




# INVESTOR MEETING 2012





# **BIG Or small...**

*It's All About The Details*

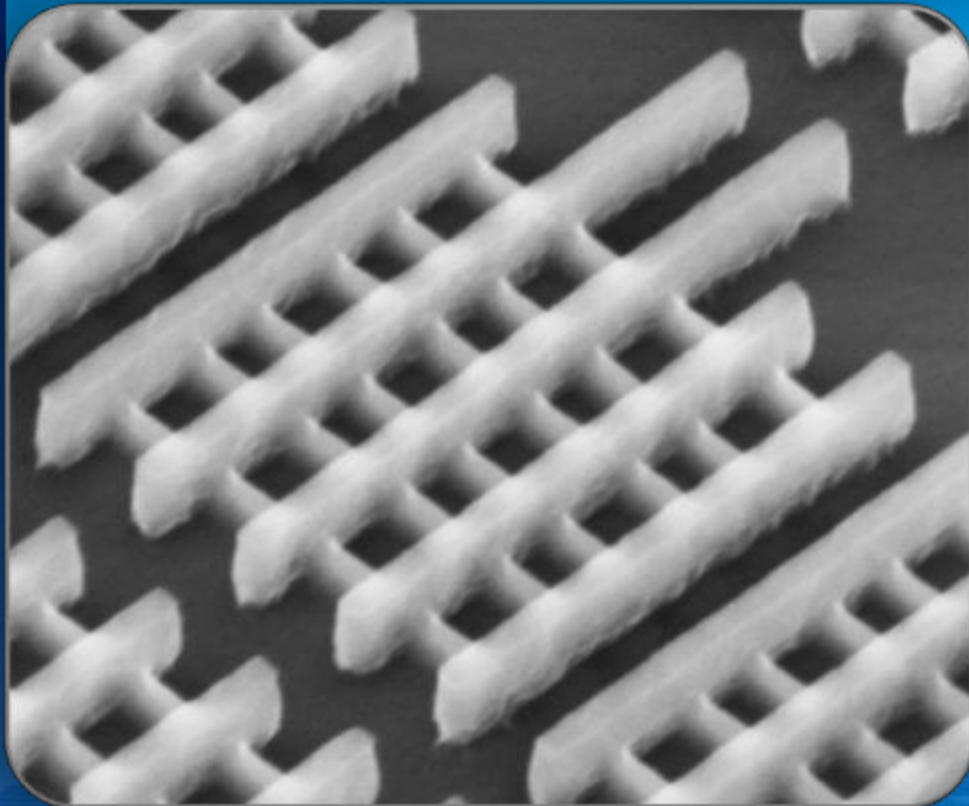
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## **Brian Krzanich**

*Senior Vice President  
Chief Operating Officer*

# Delivering The Details

Tiny Transistors,  
*Big Impact*



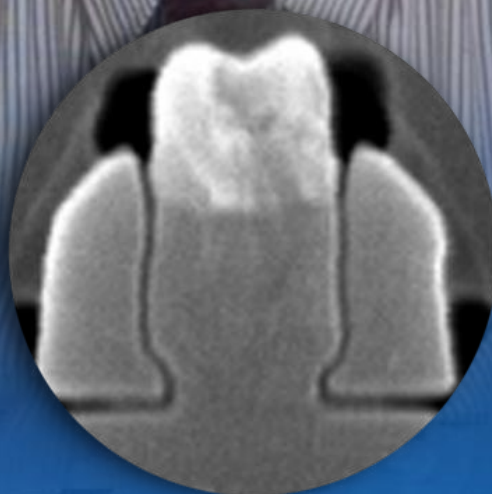
Invest Big,  
*Deliver Big*



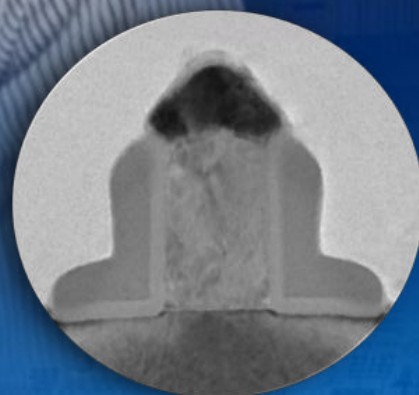


# *Predictable Silicon Track Record* **Executing to Moore's Law**

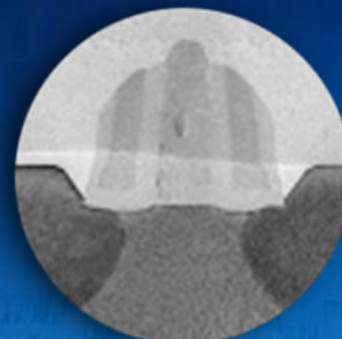
*Enabling new devices with higher functionality & complexity while controlling power, cost, and size*



180 nm  
**1999**



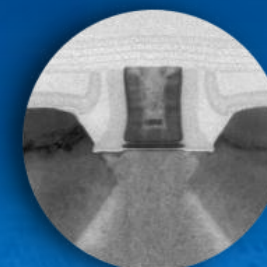
130 nm  
**2001**



90 nm  
**2003**



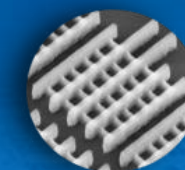
65 nm  
**2005**



45 nm  
**2007**



32 nm  
**2009**



22 nm  
**2011**

*Having fun with*  
**22nm Tri-Gate**



**>100 Million**

*22nm Tri-Gate Transistors  
would fit on the head of a pin*

A pin head is about 1.5 mm in diameter.

*Having fun with*  
**22nm Tri-Gate**

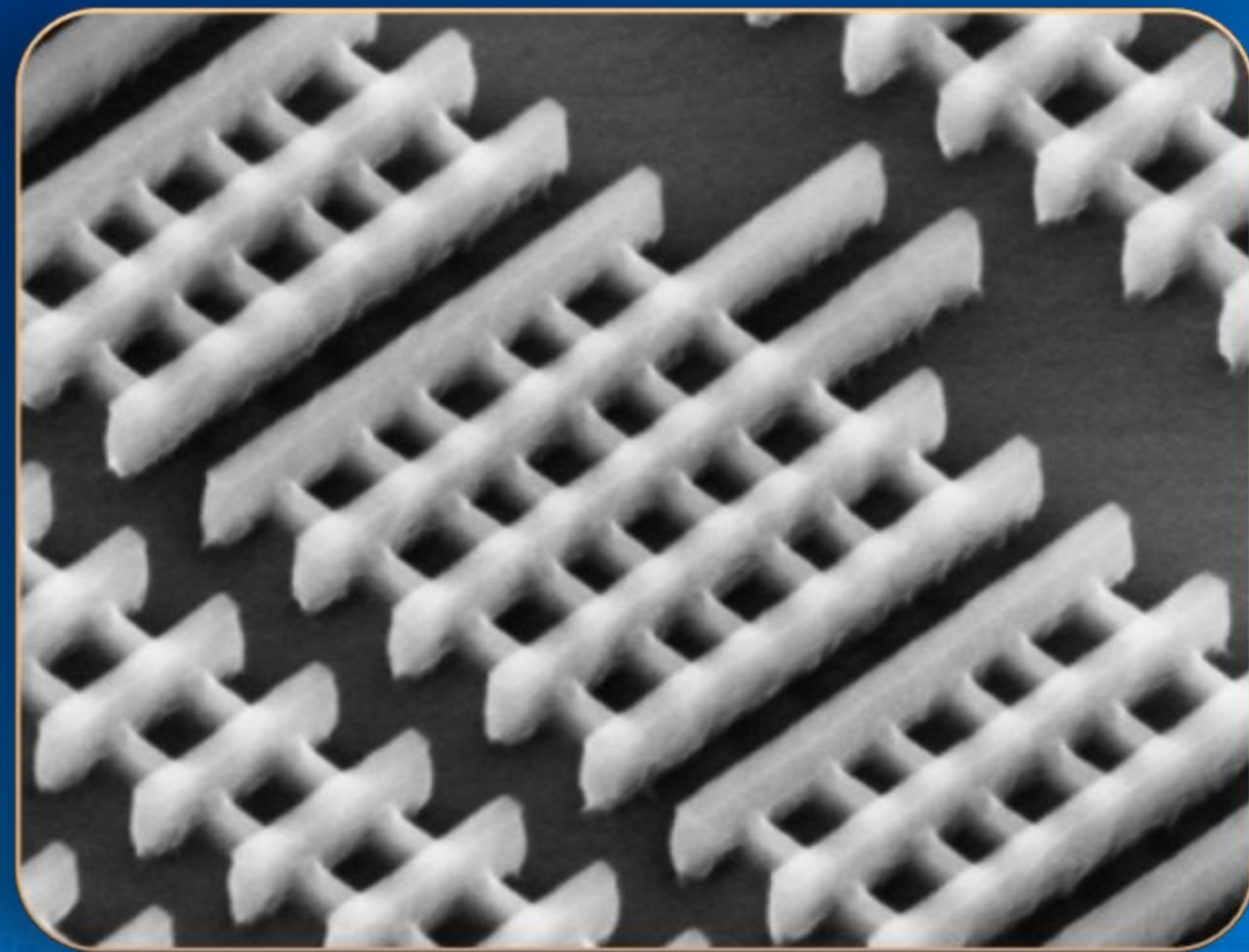


A 22nm transistor can switch on and off  
**>100 Billion Times / Second**

It would take you around  
**2000 Years to Do It**

# Mark Bohr

*Intel Senior Fellow, Technology and Manufacturing Group  
Director, Process Architecture and Integration*



# *Brian Krzanich*

*Upsized the same amount as the transistors on stage.*

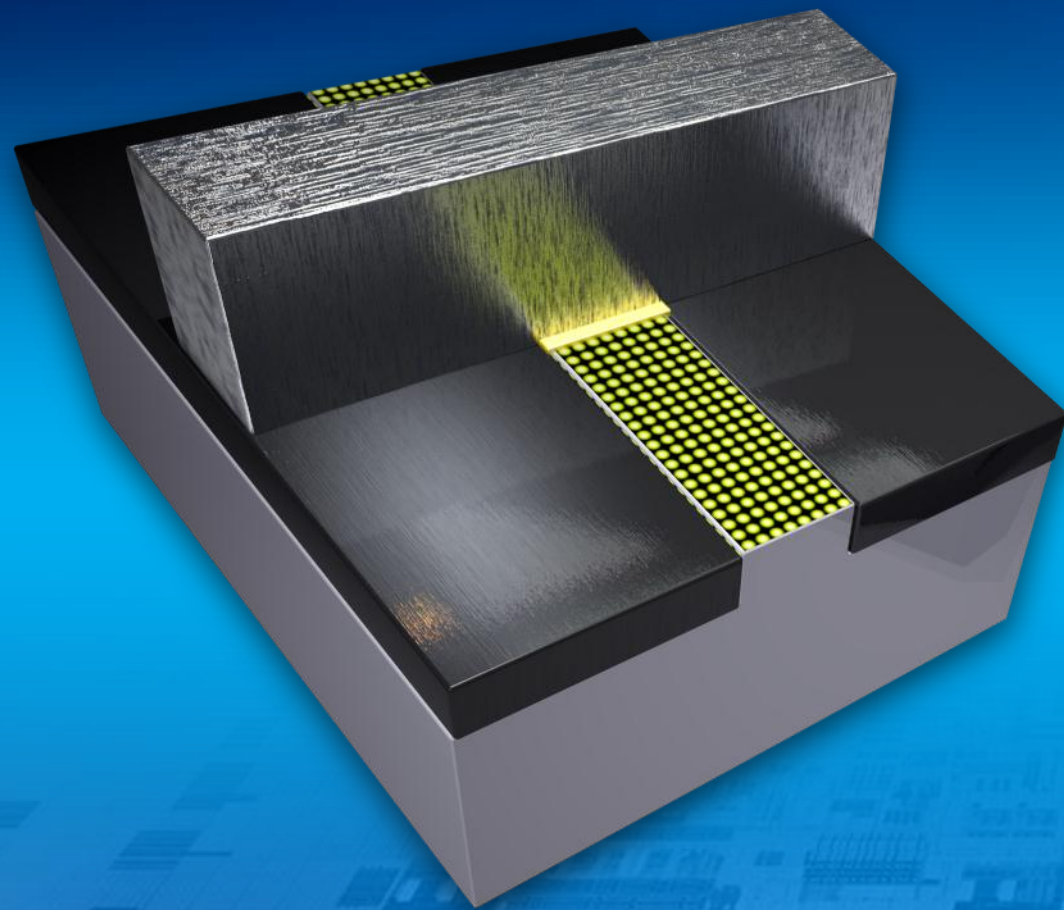




# 32nm

## *Planar Transistor*

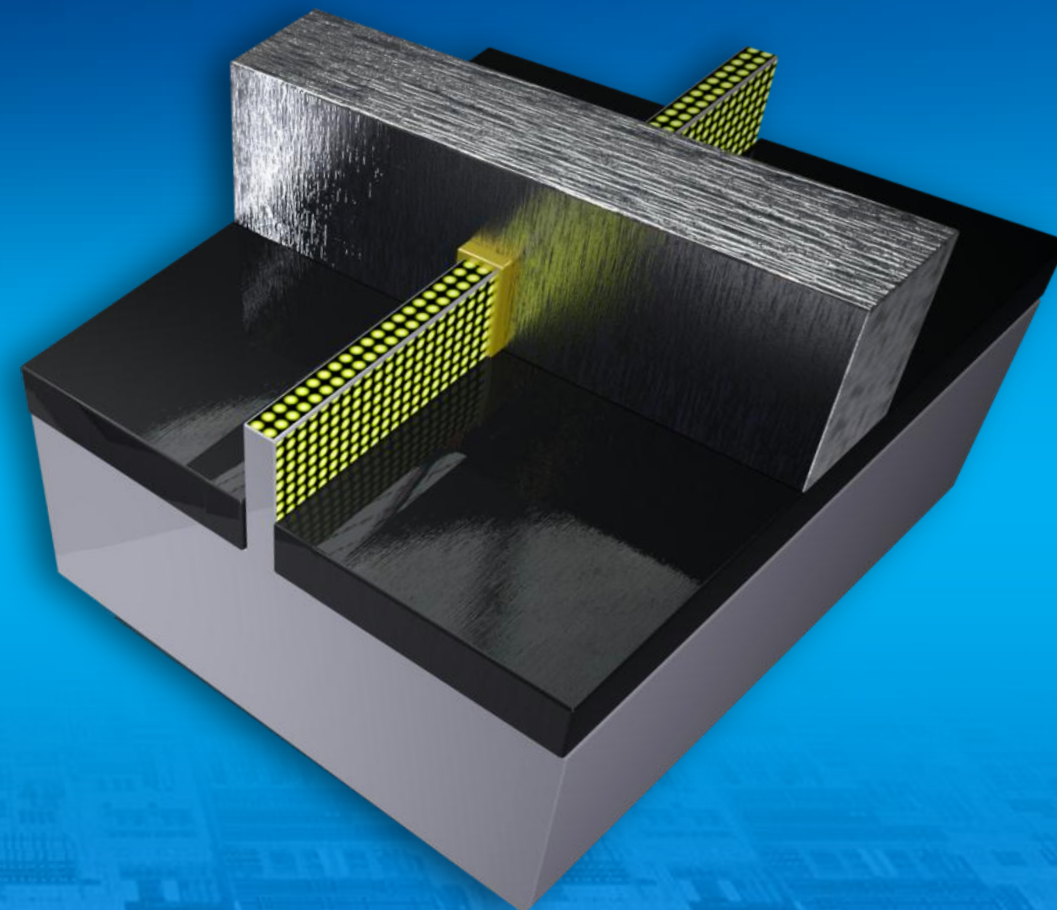
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# 22nm

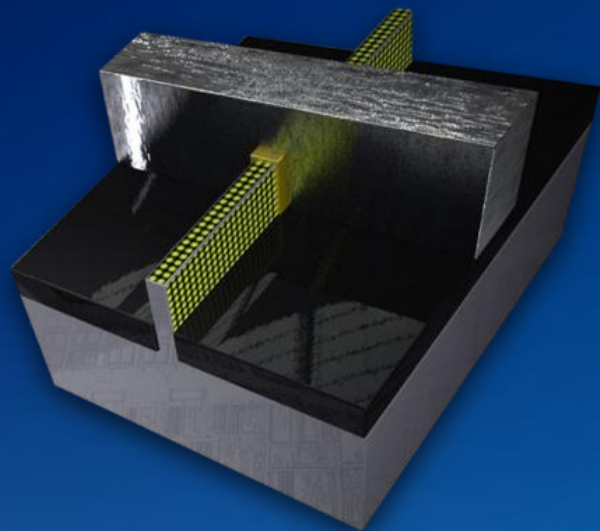
## *Tri-Gate Transistor*

---



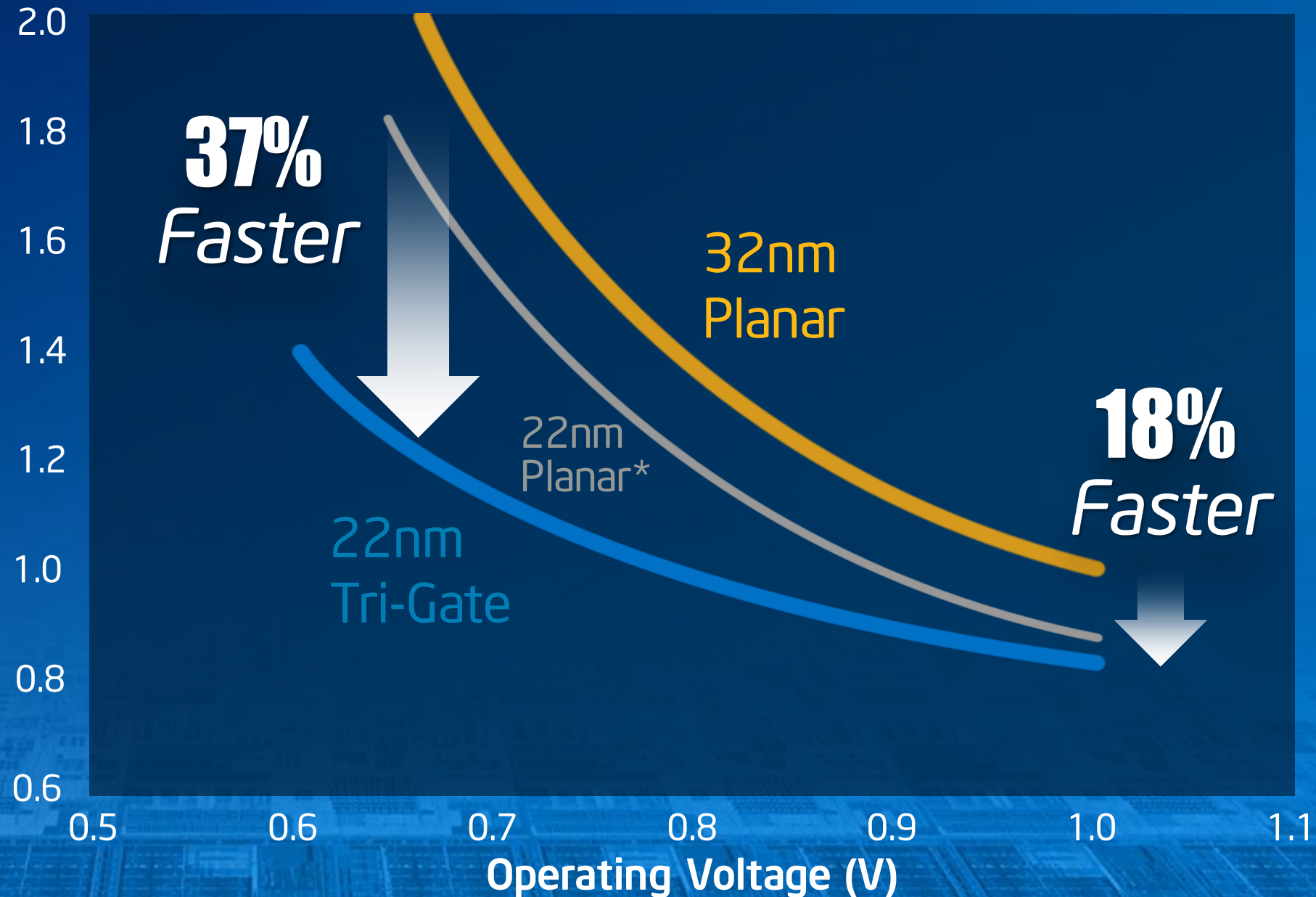
# Tri-Gate TRANSISTOR

Performance



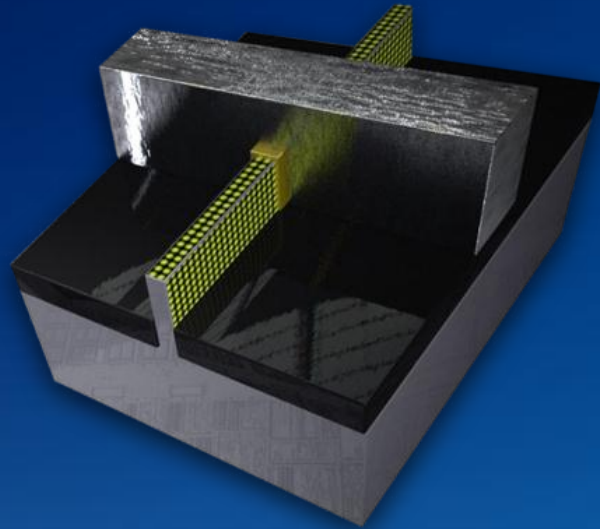
**>30%**  
Performance Increase  
at Low Voltages

Transistor  
Gate Delay



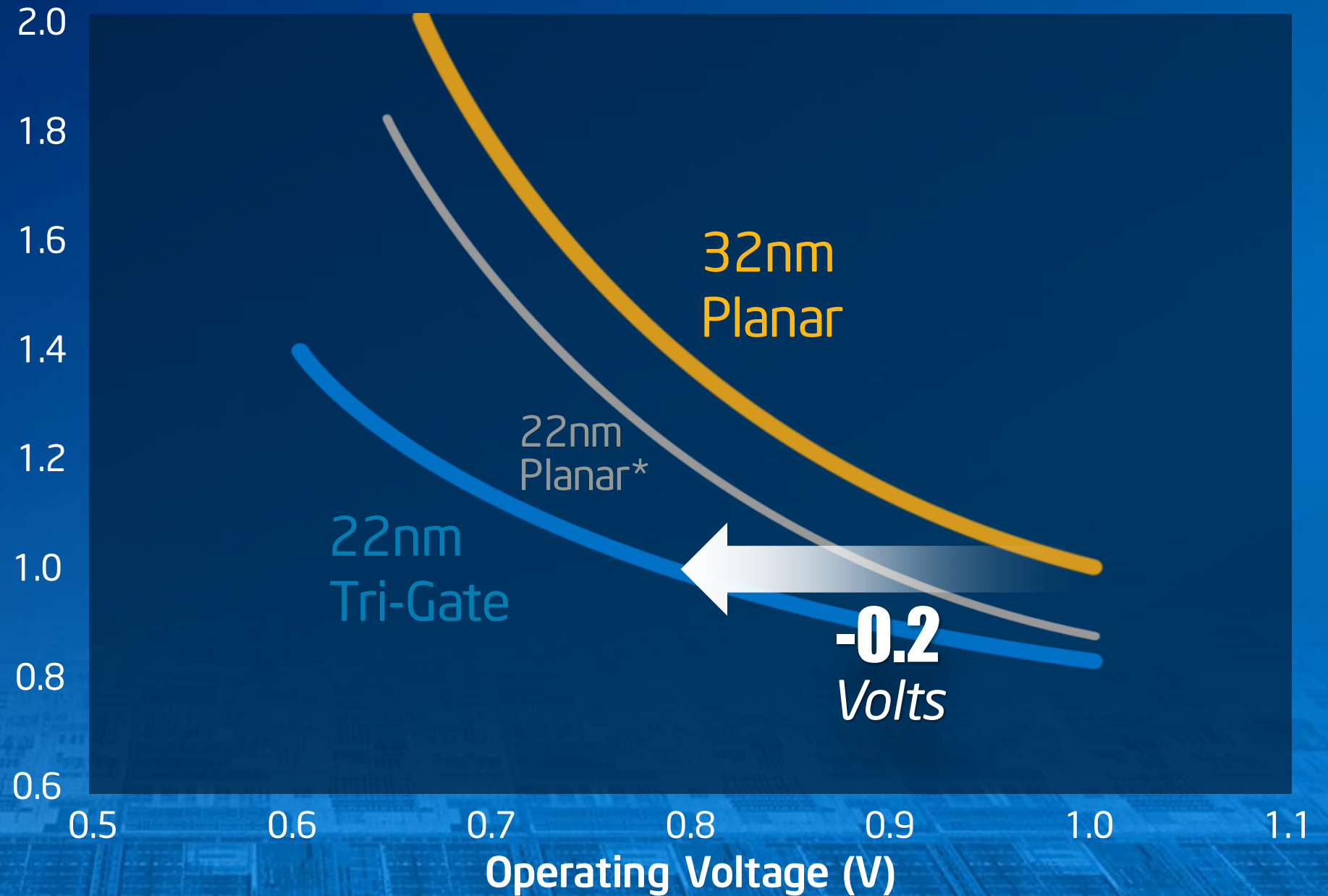
# Tri-Gate TRANSISTOR

## Performance



**~50%**  
Lower Power at  
Constant Performance

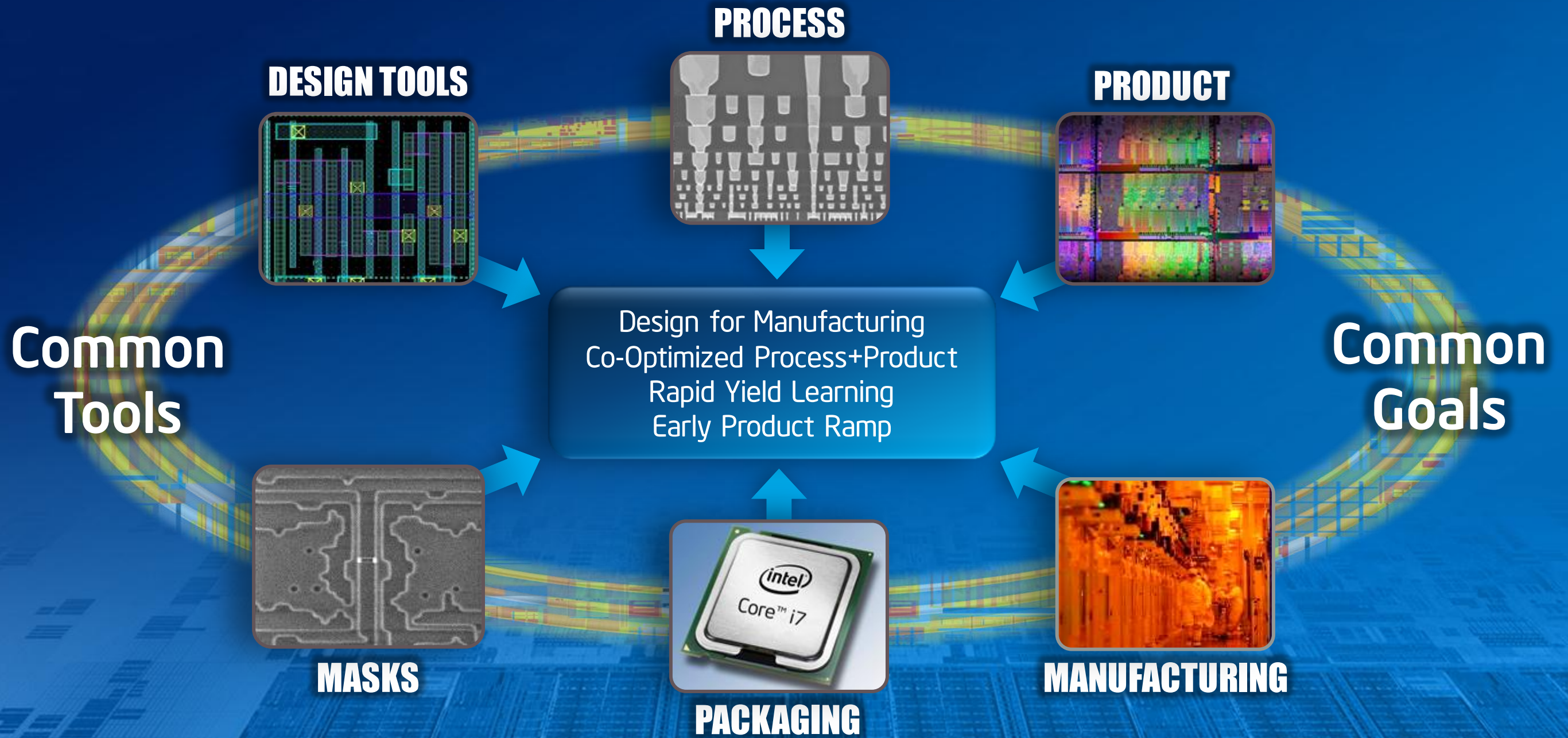
Transistor  
Gate Delay



# Moore's Law Requires More Than Just Scaling



# Intel's Increasingly Unique IDM Advantage



# The End of Scaling is Near?

*(Decades of Predictions)*

“Optical lithography can’t do sub-micron”

“Optical lithography will reach its limits in the range of 0.75-0.50 microns”

“Optical lithography should reach its limits in the 1990-1994 period”

“X-ray lithography will be needed below 1 micron”

“Minimum geometries will saturate in the range of 0.3 to 0.5 microns”

“Channel lengths can be reduced to approximately 0.2 microns”

“Minimum gate oxide thickness is limited to ~2 nm”

“Oxide reliability may limit oxide scaling to 2.2 nm”

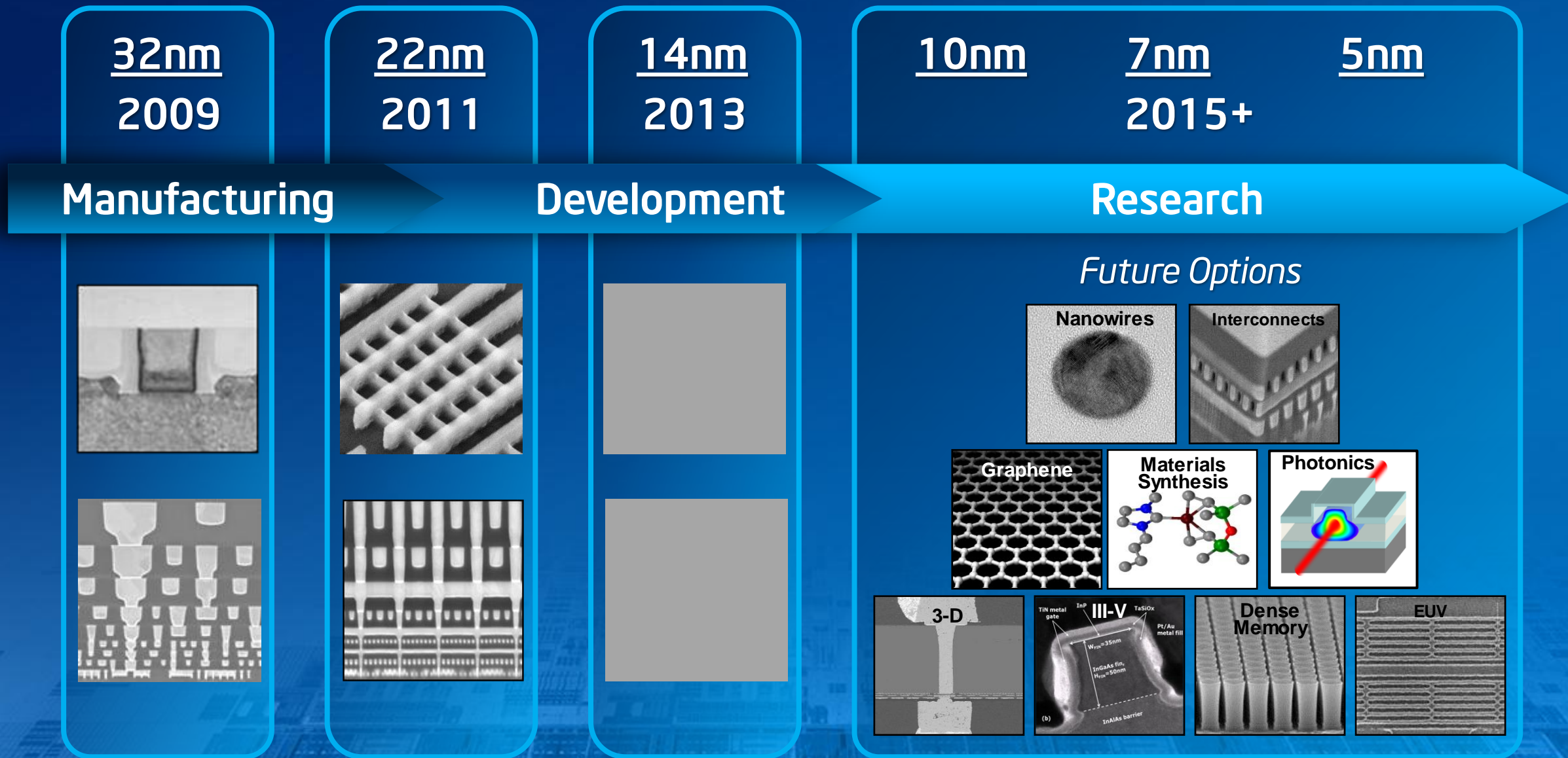
“Copper interconnects will never work”

“Plasma etched aluminum will not happen in our lifetime”

“Scaling will end in ~10 years”

# Innovation Enabled Technology Pipeline

*Our Visibility Continues to Go Out ~10 Years*



Future options subject to change

# Worldwide Scale and Growing Intel's Fab and Assembly Locations

**4M sq ft**  
Manufacturing Space

**\$36.5B**  
Cumulative Fab Investment

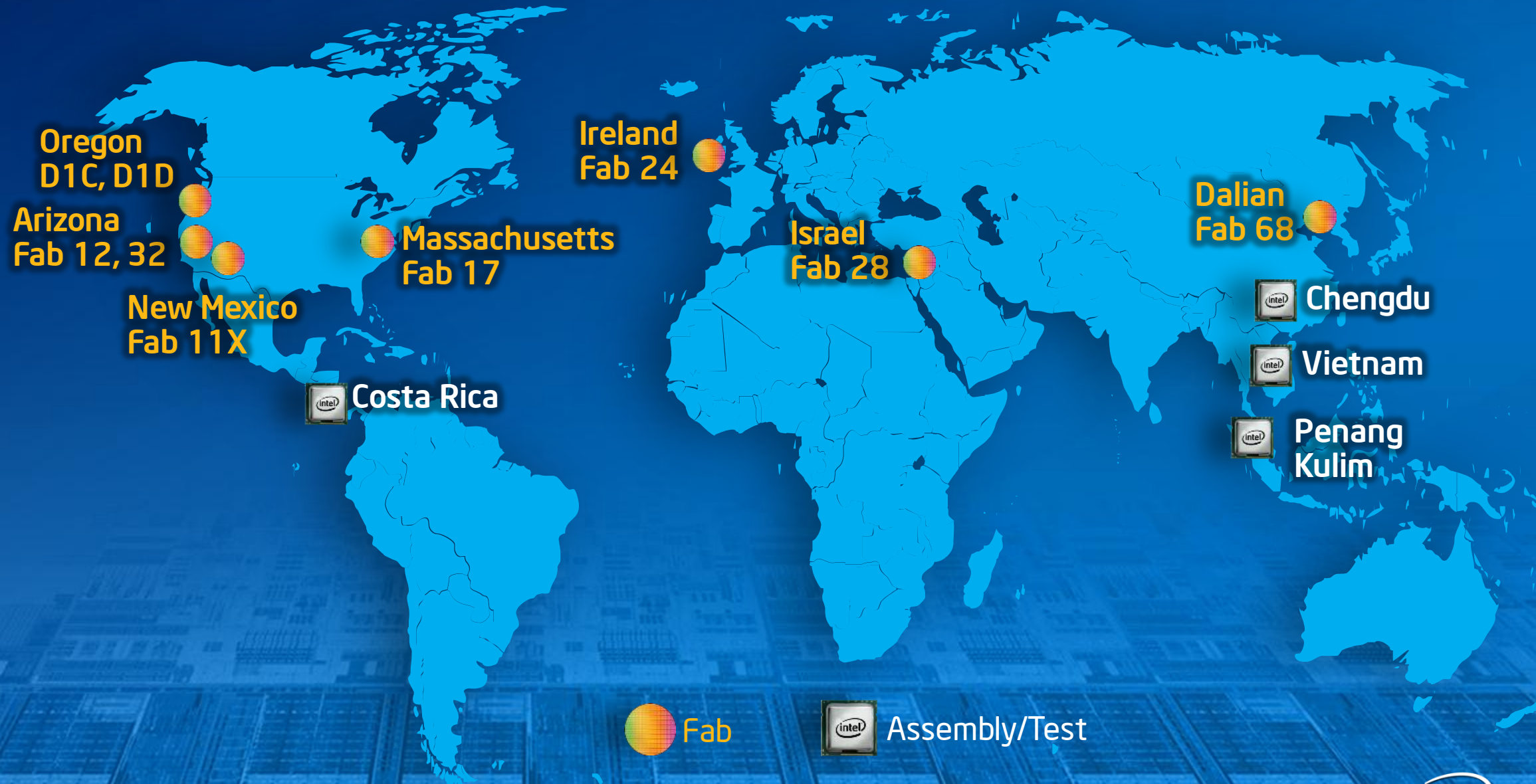
**\$4B**  
**CONSTRUCTION**



D1X - OR



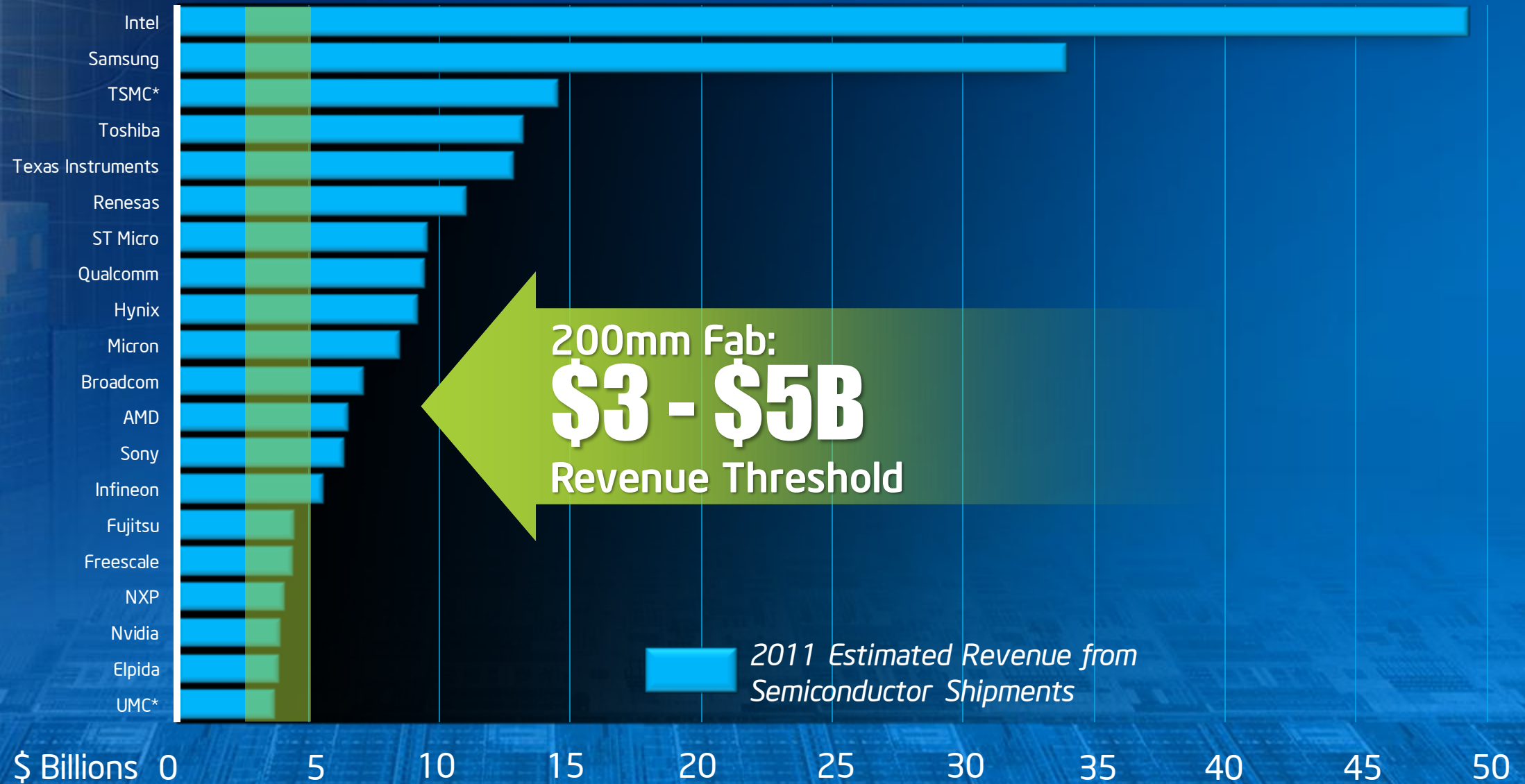
Fab 42 - AZ





# Fewer Companies Deliver Moore's Law

Semiconductor Revenue Required To Support One Leading Edge Fab



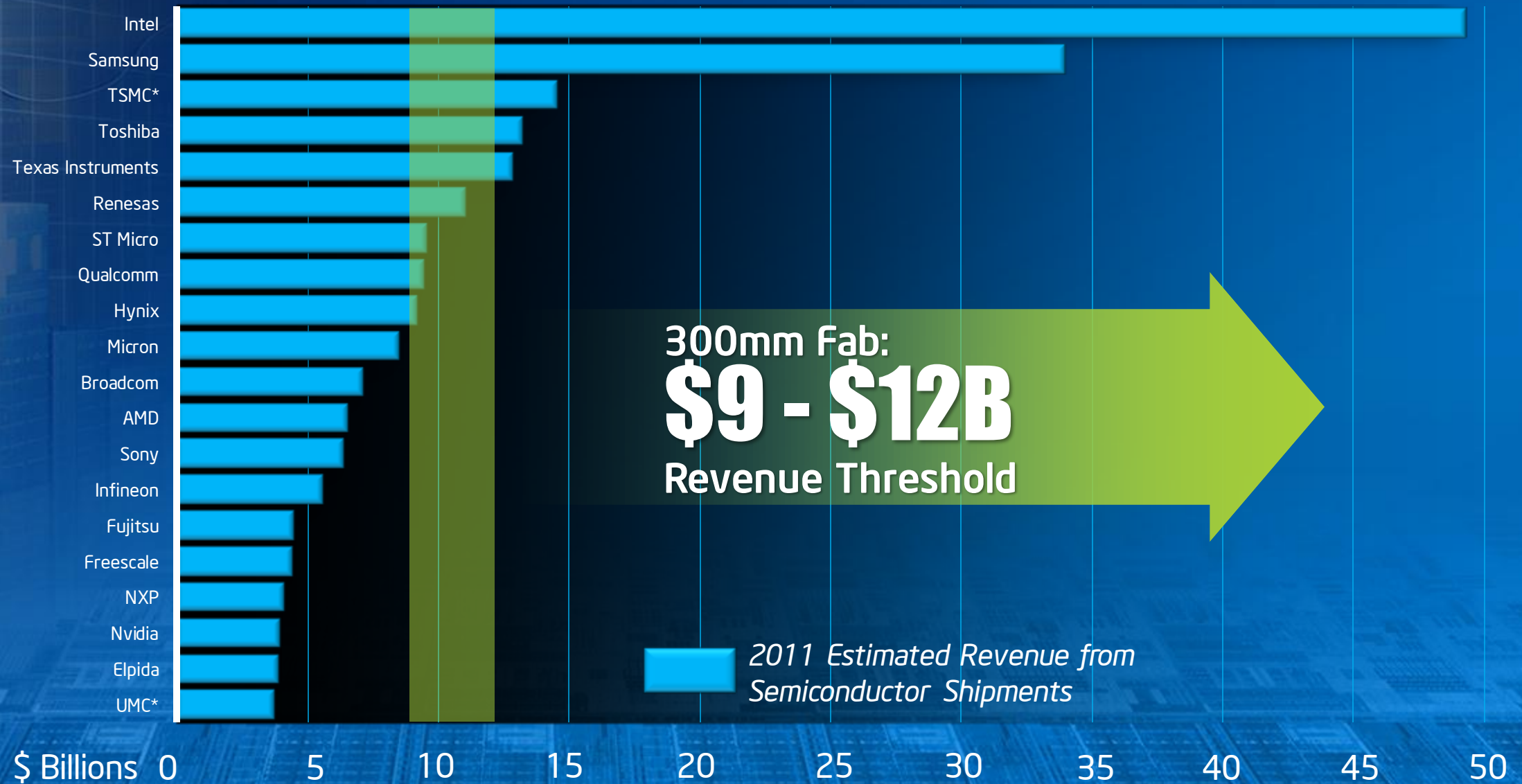
200mm Fab:  
**\$3 - \$5B**  
Revenue Threshold

2011 Estimated Revenue from Semiconductor Shipments

\*TSMC and UMC are foundries. Revenue thresholds are theoretical estimates. Assumptions include 40% and 50% gross margins. Source: IC Insights, Intel.

# Fewer Companies Deliver Moore's Law

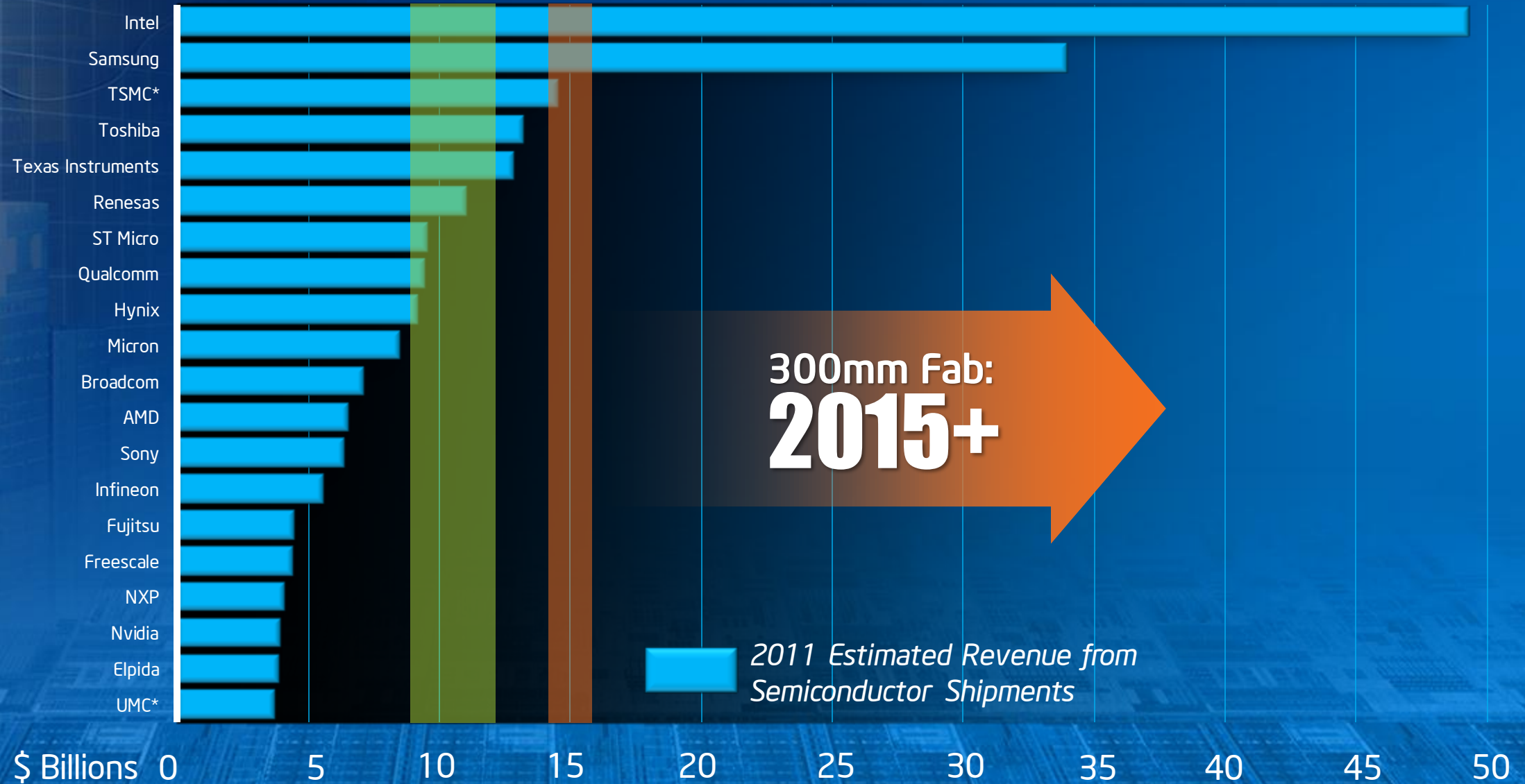
Semiconductor Revenue Required To Support One Leading Edge Fab



\*TSMC and UMC are foundries. Revenue thresholds are theoretical estimates. Assumptions include 40% and 50% gross margins. Source: IC Insights, Intel.

# Fewer Companies Deliver Moore's Law

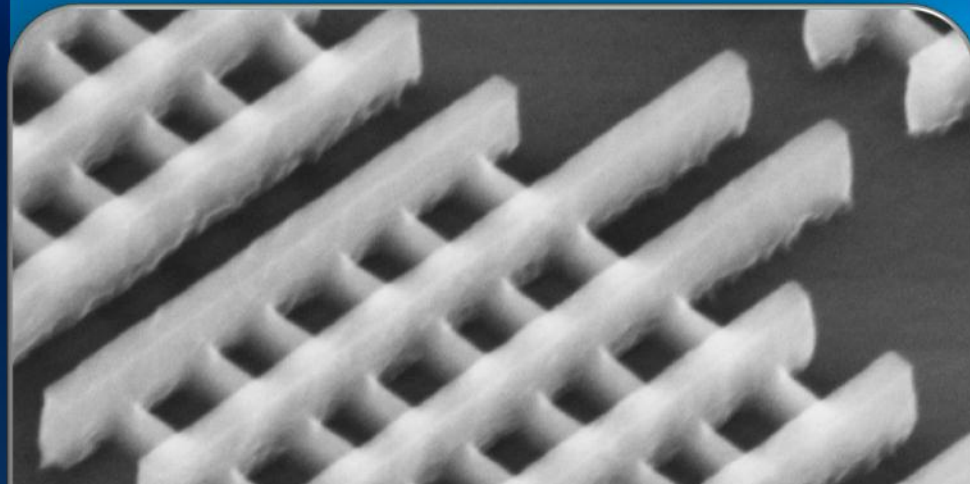
Semiconductor Revenue Required To Support One Leading Edge Fab



\*TSMC and UMC are foundries. Revenue thresholds are theoretical estimates. Assumptions include 40% and 50% gross margins. Source: IC Insights, Intel.

# Delivering The Details

Tiny Transistors,  
*Big Impact*



**We are continuing to extend our technology leadership through innovation**

Invest Big,  
*Deliver Big*



**We are making significant investments and have the scale to deliver**

# Risk Factors

The above statements and any others in this document that refer to plans and expectations for the second quarter, the year and the future are forward-looking statements that involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "plans," "believes," "seeks," "estimates," "may," "will," "should" and their variations identify forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Many factors could affect Intel's actual results, and variances from Intel's current expectations regarding such factors could cause actual results to differ materially from those expressed in these forward-looking statements. Intel presently considers the following to be the important factors that could cause actual results to differ materially from the company's expectations. Demand could be different from Intel's expectations due to factors including changes in business and economic conditions, including supply constraints and other disruptions affecting customers; customer acceptance of Intel's and competitors' products; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers. Uncertainty in global economic and financial conditions poses a risk that consumers and businesses may defer purchases in response to negative financial events, which could negatively affect product demand and other related matters. Intel operates in intensely competitive industries that are characterized by a high percentage of costs that are fixed or difficult to reduce in the short term and product demand that is highly variable and difficult to forecast. Revenue and the gross margin percentage are affected by the timing of Intel product introductions and the demand for and market acceptance of Intel's products; actions taken by Intel's competitors, including product offerings and introductions, marketing programs and pricing pressures and Intel's response to such actions; and Intel's ability to respond quickly to technological developments and to incorporate new features into its products. Intel is in the process of transitioning to its next generation of products on 22nm process technology, and there could be execution and timing issues associated with these changes, including products defects and errata and lower than anticipated manufacturing yields. The gross margin percentage could vary significantly from expectations based on capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; changes in revenue levels; segment product mix; the timing and execution of the manufacturing ramp and associated costs; start-up costs; excess or obsolete inventory; changes in unit costs; defects or disruptions in the supply of materials or resources; product manufacturing quality/yields; and impairments of long-lived assets, including manufacturing, assembly/test and intangible assets. The tax rate expectation is based on current tax law and current expected income. The tax rate may be affected by the jurisdictions in which profits are determined to be earned and taxed; changes in the estimates of credits, benefits and deductions; the resolution of issues arising from tax audits with various tax authorities, including payment of interest and penalties; and the ability to realize deferred tax assets. Gains or losses from equity securities and interest and other could vary from expectations depending on gains or losses on the sale, exchange, change in the fair value or impairments of debt and equity investments; interest rates; cash balances; and changes in fair value of derivative instruments. The majority of Intel's non-marketable equity investment portfolio balance is concentrated in companies in the flash memory market segment, and declines in this market segment or changes in management's plans with respect to Intel's investments in this market segment could result in significant impairment charges, impacting restructuring charges as well as gains/losses on equity investments and interest and other. Intel's results could be affected by adverse economic, social, political and physical/infrastructure conditions in countries where Intel, its customers or its suppliers operate, including military conflict and other security risks, natural disasters, infrastructure disruptions, health concerns and fluctuations in currency exchange rates. Expenses, particularly certain marketing and compensation expenses, as well as restructuring and asset impairment charges, vary depending on the level of demand for Intel's products and the level of revenue and profits. Intel's results could be affected by the timing of closing of acquisitions and divestitures. Intel's results could be affected by adverse effects associated with product defects and errata (deviations from published specifications), and by litigation or regulatory matters involving intellectual property, stockholder, consumer, antitrust, disclosure and other issues, such as the litigation and regulatory matters described in Intel's SEC reports. An unfavorable ruling could include monetary damages or an injunction prohibiting Intel from manufacturing or selling one or more products, precluding particular business practices, impacting Intel's ability to design its products, or requiring other remedies such as compulsory licensing of intellectual property. A detailed discussion of these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent Form 10-Q, Form 10-K and earnings release.



# INVESTOR MEETING 2012

