Allwinner Technology

A20

Datasheet

Revision 1.0
Feb 27, 2013

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Revision History

Revision	Date	Author	Description
1.0	2013.02.27	Allwinner	Initial Version

1 OVERVIEW

Allwinner A20 processor is a dual-core ARM Cortex-A7 mobile application solution designed for tablet and smart TV applications.

A20 processor is based on a dual-core ARM Cortex-A7 CPU architecture, which is the most energy efficient application processor from ARM so far and incorporates all the features of Cortex-A15. It also integrates the powerful ARM Mali400 MP2 GPU, delivering a reliable system performance as well as good game compatibility. Besides, A20 supports 2160p video decoding and H.264 HP 1080p video encoding.

Additionally, A20 processor features a wide range of interfaces and connectivity, including 4-CH CVBS in, 4-CH CVBS out, HDMI with HDCP, VGA, LVDS/RGB LCD, SATA, USB, and GMAC, etc. More importantly, A20 processor is pin-compatible with its predecessor A10, which greatly simplifies the product design process and makes the upgrade of a design much easier.

2 FEATURE

Dual-Core CPU

- Dual Cortex-A7
  - –ARMv7 ISA standard ARM instruction set
  - –Thumb-2
  - –Jazeller RCT
  - –NEON Advanced SIMD
  - –VFPv4 floating point
  - –Hardware virtualization support
  - –Large Physical Address Extensions(LPAE)
  - –JTAG debug
  - –One general timer for individual CPU
  - –32KB Instruction and 32KB Data L1 Cache for individual CPU

Graphic Engine

- 3D
  - –Mali400 MP2 GPU
  - –Support OpenGL ES 2.0 / OpenVG 1.1 standard
- 2D
  - –Support BLT and ROP2/3/4
  - –Support 90° /180° /270° rotation
  - –Support mirror/ alpha (plane and pixel alpha) / color key
  - –Format conversion: ARGB 8888/4444/1555, RGB565, MONO 1/2/4/8bpp, Palette 1/2/4/8bpp (input only), YUV 444/422/420

Memory

- Internal BROM
  - –Support system boot from NAND Flash, SPI Nor Flash (SPI0), SD Card/TF card (SDC0/2)
  - –Support system code download through USB OTG (USB0)
- SDRAM
  - –Support DDR3/DDR3L/DDR2
  - –Support 32-bit bus width
  - –Support 2GB address space
- NAND Flash
  - –Comply to ONFI 2.3 and Toggle 1.0
  - –Support 64 bits ECC per 512 bytes or 1024 bytes
  - –Support 8bits data bus width
  - –Support 1.8V/3.3V signal voltage
  - –Support 1K/2K/4K/8K/16K page size
  - –Support up to 8 CE and 2 RB
  - –Support system boot from NAND flash
  - –Support SLC/MLC NAND and EF-NAND
  - –Support SDR/DDR NAND interface
- SD/MMC Interface
  - –Comply with eMMC standard specification V4.3
  - –Comply with SD physical layer specification V3.0
  - –Comply with SDIO card specification V2.0
  - –Support 1/4/8 bits bus width
  - –Support HS/DS/SDR12/SDR25 bus mode
  - –Support eMMC mandatory and alternative boot operations
  - –Support four independent SD/MMC/SDIO controllers
  - –Support SDSC/SDHC/SDXC/MMC/ RS-MMC card
  - –Support eMMC/iNand Flash
  - –Support 1GB/2GB/4GB/8GB/16GB/32GB/64GB /128GB SD/MMC card
  - –Support SDIO interrupt detection
  - –Support descriptor-based internal DMA controller for efficient scatter and gather operations

System Resources

- **Timer**
  - –6 timers: clock source can be switched over 24M/32K for all timers, and external signals can be used as clock source for Timer4/5
  - –Two 33-bit AVS counters
  - –Watchdog to generate reset signal or interrupt
  - –Real time counter for second, minute, hour, day, month, and year
- **High Speed Timer**
  - –4 channels
  - –Clock source is fixed to AHB, and the pre-scale ranges from 1 to 16
  - –56-bit counter that can be separated to 24-bit high register and 32-bit low register
- **DMA**
  - –16 channels
  - –Support data width of 8/32 bits
  - –Support linear and IO address modes
- **CCU**
  - –8PLLs, a main 24MHz oscillator, an on-chip RC oscillator and a 32768Hz oscillator (optional)
- **GIC**
  - –Support 16 SGIs, 16 PPIs, and 128 SPIs
  - –Support ARM architecture security extensions
  - –Support ARM architecture virtualization extensions
  - –Support uniprocessor and multiprocessor environments

Video Engine (Phoenix 3.0)

- Video Decoding
  - –Support picture size up to 3840x2160
  - –Support decoding speed up to 1080p@60fps
  - –Supported formats: Mpeg1/2, Mpeg4 SP/ASP GMC, H.263 including Sorenson Spark, H.264 BP/MP/HP, VP6/8, AVS jizun, Jpeg/Mjpeg, etc.
- Video Encoding
  - –H.264 HP up to 1080p@30fps
  - –Jpeg baseline: picture size up to 4080x4080
  - –Alpha blending
  - –Thumb generation
  - –4x2 scaling ratio from 1/16 to 64 arbitrary non-integer ratio

Display Engine

- Four moveable and size-adjustable layers, each layer size up to 8192x8192 pixels
- Ultra-Scaling engine
  - –8-tap scale filter in horizontal and 4 tap in vertical
  - –Source image size from 8x4 to 8192x8192 resolution and destination image size from 8x4 to 8192x8192 resolution
- Support multiple image input formats
  - –mono 1/2/4/8 bpp
  - –palette 1/2/4/8 bpp
  - –6/24/32 bpp color
  - –YUV444/420/422/411
- Support alpha blending/color key/gamma/harware cursor/sprite
- Output color correction: luminance/hue/saturation, etc
- Support de-interlace
- Video enhancement: lum peaking/DCTi/black and white level extension
- 3D input/output format conversion and display

Video Output

- HDMI 1.4 transmitter with HDCP
- LVDS/Sync RGB/CPU LCD interface up to 1920x1200 resolution
- Support 4-channel CVBS, or 2-channel S-video, or 1-channel YPbPr/VGA (YPbPr/VGA up to 1080p)
- Support two-channel independent display

Video Input

- Support TV decoder: 4-ch analog CVBS or 1-ch YPbPr(480i/576i/480p/576p) signal input
- Dual CMOS sensor parallel interfaces that support YUV format only
  - –CSI0 up to 1080p@30fps
  - –CSI1 up to 720p@30fps
- Support BT656 interface
- Support 24-bit YUV444/RGB interface

Analog Audio Output

- Stereo audio DAC
- Stereo capless headphone drivers
  - –Up to 100dB SNR during DAC playback
  - –Support 8KHz~192KHz DAC sample rate
- One low-noise analog microphone bias
- Dedicated headphone outputs
- Two mixers to meet different requirements
  - –Output mixer for LINEINL/R, FMINL/R, MIC1/2 and Stereo DAC output
  - –ADC record mixer for LINEINL/R, FMINL/R, MIC1/2 and Stereo DAC output

Analog Audio Input

- Support four analog audio inputs
  - –Two microphone inputs
  - –Differential or stereo line-in input
  - –Stereo FM-in input
- Stereo audio ADC
  - –96dBA SNR
  - –Support 8KHz ~ 48KHz ADC sample rate

RTP

- 12-bit SAR ADC
- Dual touch detection
- Sampling frequency up to 2MHz

Connectivity

- **USB2.0 OTG**
  - –Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
  - –Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
  - –Support up to 5 user-configurable endpoints for Bulk , Isochronous, Control and Interrupt
- **USB EHCI/OHCI**
  - –Two EHCI/OHCI-compliant hosts
- **EMAC**
  - –Support 10/100Mbps MII data transfer rate
- **GMAC**
  - –Comply with the IEEE 802.3-2002 standard
  - –Programmable frame length to support Standard or Jumbo Ethernet frames with size up to 16KB
  - –Support 10/100/1000Mbps data transfer rates RGMII interface to communicate with an external Gigabit PHY
  - –Support 10/100Mbps MII PHY interface
- **Digital Audio In/Out**
  - –One I2S compliant audio interface, supporting 8-channel and 2-channel input
  - –One PCM, supporting linear sample(8-bit or 16-bit), 8-bit u-law and A-law companded sample
  - –One AC97 audio codec, supporting 2-channel and 6-channel audio data output
- **Transport Stream Controller**
  - –Support both SPI and SSI
  - –Speed up to 150Mbps for both SPI and SSI
  - –Support 32-channel PID filter
  - –Support hardware PCR packet detect
- **Open-Drain TWI**
  - –Up to 5 TWIs compliant with TWI protocol
- **Smart Card Reader**
  - –One smart card reader controller supporting ISO/IEC 7816-3 and EMV2000 specifications
  - –Support synchronous and any other non-ISO 7816 and non-EMV cards
- **SPI**
  - –Master/Slave configurable
  - –Up to 4 independent SPI controllers: SPI0 with one CS signal for system boot, SPI1/2/3 each with two CS signals
- **UART**
  - –Up to 8 UART controllers:UART0 with two wires for debug tools, UART1 with 8 wires, UART2/3 each with 4 wires, and others each with 2 wires

- **PS2**
  - –Two PS2 compliant to IBM PS2 and AT-compatible keyboard and mouse interface
  - –Dual-role controller: a PS2 host or a PS2 device
- **IR**
  - –Two IR controllers supporting CIR, MIR and FIR modes
- **SATA**
  - –One SATA Host controller
  - –Support SATA 1.5Gb/s and SATA 3.0Gb/s
  - –Comply with SATA spec 2.6
  - –Support external SATA(eSATA)
- **CAN**
  - –One CAN bus controller
  - –Support the CAN2.0 A/B protocol specification
  - –Programmable data rate up to 1Mbps
- **Keypad**
  - –One keypad matrix interface up to 8 rows and 8 colums
  - –Interrupt for key press or key release
  - –Internal debouncing filter to prevent switching noises
- **LRADC**
  - –6-bit resolution
  - –Voltage input range between 0V to 2V
- **PWM**
  - –2 PWM outputs
  - –Support cycle mode and pulse mode
  - –The pre-scale is from 1 to 64

Security System

- Security System
  - –Support AES, DES, 3DES, SHA-1, MD5
  - –Support ECB/CBC/CNT modes for AES/DES/3DES
  - –128-bit, 192-bit and 256-bit key size for AES
  - –160-bit hardware PRNG with 192-bit seed
- Security JTAG

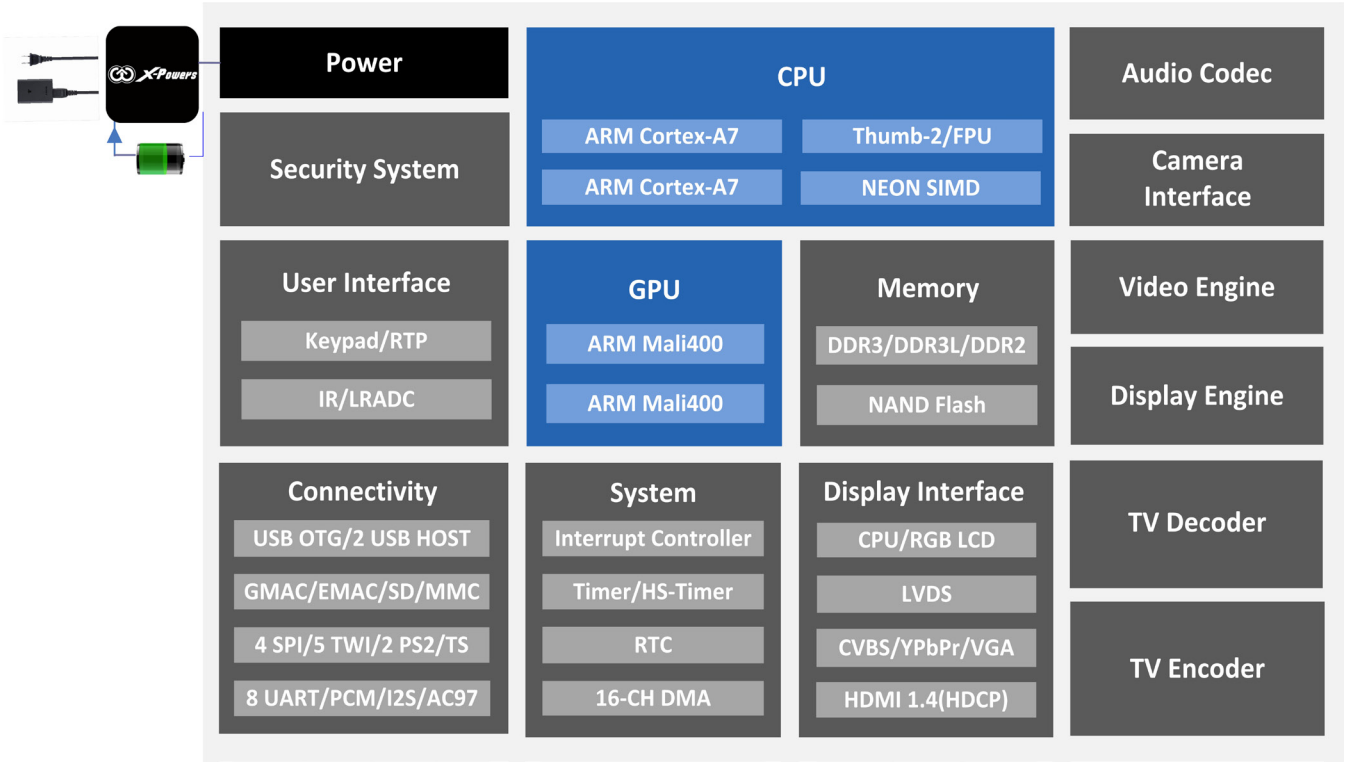
Power Management

- Flexible PLL clock generator and OSC for 32KHz
- Flexible clock gate
- Support DVFS for CPU frequency and voltage adjustment
- Support standby mode (only DDR+RTC-Domain power exist)

Package

- FBGA 441 balls,0.80mm ball pitch, 19x19x1.4mm

3 BLOCK DIAGRAM

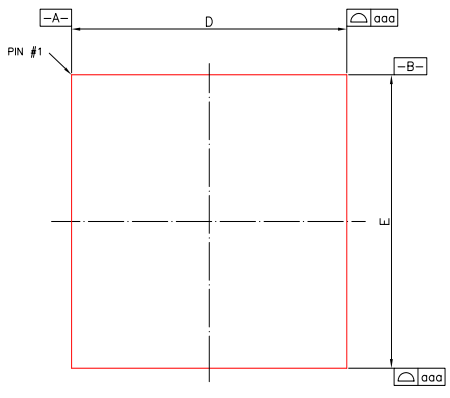


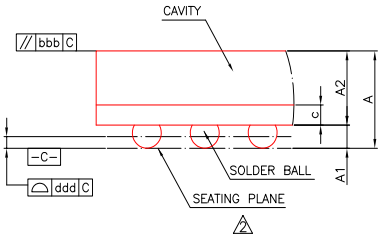
6 PIN ASSIGNMENT

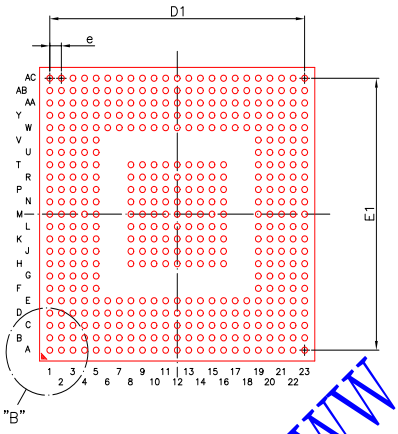
6.1. PIN MAP

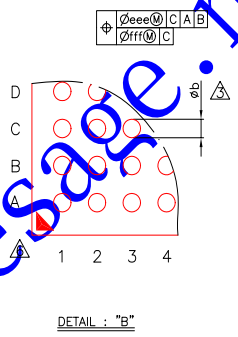
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	PH15	PH13	PH10	PH6	PH3	PH0	PB22	PB18	PB16	PB14	PB8	PB6	PB4	PB2	PB0	PI8	PI6	PI4	PI2	PI0	PE11	PE9	PE8	A
B	PH16	PH14	PH11	PH7	PH4	PH1	PB23	PB19	PB17	PB15	PB13	PB7	PB5	PB3	PB1	PI9	PI7	PI5	PI3	PI1	PE10	PE7	PE6	B
C	PH17	PH18	PH12	PH8	PH5	PH2	PB21	PB20	PB12	PB11	PB10	PB9	PA17	RESET#	PI14	PI12	PI10	PG11	PG9	PG7	PG5	PE5	PE4	C
D	PH19	PH20	PH21	PH9	PA0	PA2	PA4	PA6	PA8	PA10	PA12	PA14	PA16	PI19	PI15	PI13	PI11	PG10	PG8	PG4	PG3	PE3	PE2	D
E	PH22	PH23	PH24	PH25	PA1	PA3	PA5	PA7	PA9	PA11	PA13	PA15	PI21	PI20	PI18	PI17	PI16	VCC-PG	PG6	PG2	PG1	PE1	PE0	E
F	X32KI	X32KO	PH26	PH27	NMI#														VCC-PE	PG0	PC24	PC18	PC17	F
G	SDQM3	SDQ29	GND	GND	VCC-DRAM														PC23	PC15	PC14	PC11	PC10	G
H	SDQ26	SDQ31	SVREF	SVREF	VCC-DRAM			VCC	VCC	VCC-PA	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	VCC	TEST			VCC-PC	PC13	PC12	PC9	PC8	H
J	SDQ24	SDQS3B	SCK1B	SCK1	GND			VCC	VCC	VCC-PA	GND	VDD-CPU	VDD-CPU	VCC	VDD-SYS	VDD-SYS			VCC-PC	PC22	PC21	PC7	PC6	J
K	SDQS3	SDQ27	SBA0	SBA2	GND			VDD-RTC	VDD-SYS	VDD-SYS	GND	GND	GND	GND	VDD-SYS	VDD-USB			PF5	PF4	PC20	PC5	PC4	K
L	SDQ25	SDQ28	SA10	SBA1	VCC-DRAM			VDD-SYS	VDD-SYS	GND	GND	GND	GND	GND	VCC-USB	VCC-USB			PF3	PF2	PC19	PC3	PC2	L
M	SDQ30	SDQ23	SA7	SA3	VCC-DRAM			VDD-DLL	GND	GND	GND	GND	GND	GND	VDD-SATA	VDD-SATA			PF1	PF0	PC16	PC1	PC0	M
N	SDQ22	SDQ17	SCKE	SA5	GND			SADBG	VDD-DLL	GND	GND	GND	GND	GND	VDD25-SATA	VDD25-SATA			VCC-PF	DM0	DP0	X24MO	X24MI	N
P	SDQ19	SDQS2B	SA12	SA9	GND			SDDBG0	VDD-DLL	GND	GND	GND	GND	GND	GND	VCC-PLL			SATA-CLKM	DM1	DP1	HHPD	HCEC	P
R	SDQS2	SDQM2	SA14	SA1	VCC-DRAM			SDDBG1	VDD-SYS	VDD-SYS	GND	GND	GND	NC	PLLVREG	NC			SATA-CLKP	DM2	DP2	HSDA	HSCL	R
T	SDQ20	SDQ16	SWE	SRAS	VCC-DRAM			VDD-SYS	VDDQE	JTAG-SEL	GND	GND	VCC-HMDI	HVREG1	PLLTEST	PLLDV			AVCC	SATA-TXP	SATA-TXM	HTX2N	HTX2P	T
U	SDQ21	SDQ18	SCAS	SA2	GND														AGND	SATA-RXM	SATA-RXP	HTX1N	HTX1P	U
V	SCK	SCKB	SCS	SA6	GND														GND-HP	VRA2	REXT-SATA	HTX0N	HTX0P	V
W	SDQM1	SDQ13	SA11	SA0	VCC-DRAM	VCC-DRAM	VCC-DRAM	BOOTSEL	GND	GND	GND	VCC-LVDS	VCC-LVDS	VCC-LVDS	VCC-TVOUT	VCC-TVIN	VCC25-TVIN	GND	HPR	VRA1	VRP	HTXCN	HTXCP	W
Y	SDQ10	SDQ15	SA13	SA4	SVREF	VCC-DRAM	GND	GND	PD24	PD20	PD18	PD16	PD14	PD12	PD10	VRN-TVIN	TVIN3	GND	HPL	FMINL	FMINR	TPX1	TPY1	Y
AA	SDQ8	SDQS1B	SA8	SA15	SODT	SRST	SZQ	SVREF	PD25	PD21	PD19	PD17	PD15	PD13	PD11	VRP-TVIN	TVIN2	GND	HPCOM	HPCOMFB	VMIC	TPX2	TPY2	AA
AB	SDQS1	SDQ11	SDQ14	SDQ6	SDQ3	SDQS0	SDQ4	SDQ5	PD26	PD22	PD8	PD6	PD4	PD2	PD0	TVOUT1	TVOUT3	TVIN1	VCC-HP	LINEINL	LINEINR	LRADC1	LRADC0	AB
AC	SDQ9	SDQ12	SDQ7	SDQ1	SDQS0B	SDQM0	SDQ0	SDQ2	PD27	PD23	PD9	PD7	PD5	PD3	PD1	TVOUT0	TVOUT2	TVIN0	HPBP	MICIN1	MICIN2	MICOUTP	MICOUTN	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

6.2. PACKAGE DIMENSION









Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.22	0.26	0.30	0.009	0.010	0.012
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.60	---	---	0.693	---
E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.20			0.008		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23/23			23/23		